Sandia National Laboratories Rad Hard Microelectronics On-Board Processing

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Overview

- Rad Hard Microelectronics Strategy & Capabilities
- Focal Plane Array Microsystem
- Rad Hard Pentium Program
- Summary

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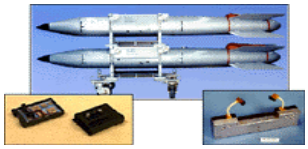
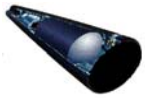
Sandia Microelectronics is driven by Systems Customers



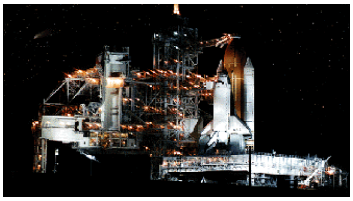
B61 Alt 339 MET Alt 325 TSSG



Warhead Life Extension Program

Nuclear Weapons

Nuclear Non-proliferation (Satellites)



Other Government

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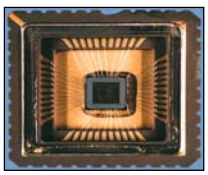
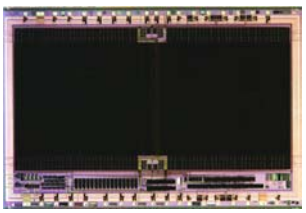
Sandia Strategy for Supplying Rad-Hard Products

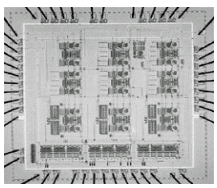
- Buy commercial parts when they meet mission requirements.
- Maintain in-house research, technology, and product capability
  - Transfer technology to willing industrial partners for manufacturing
  - Where uniquely qualified, supply products to customers from MDL
  - 75% Development, 25% Product Production



Honeywell SA 3935 Digital ASIC



SNL rad-hard NVM technology transferred to Northrop-Grumman



MDL-fabricated rad-hard analog IC

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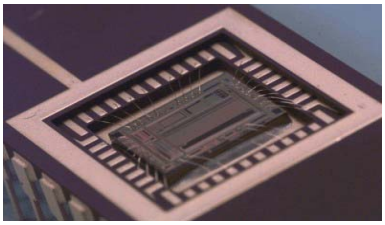
SNL Microsystems Product Infrastructure

Design
IC Layout Using Mentor ICGRAPH



Fabrication
Over 30,000 ft^2 of clean room, .35µm CMOS Fabrication Facility

Packaging
Internal Prototyping
External HR Packaging at Golden Altos

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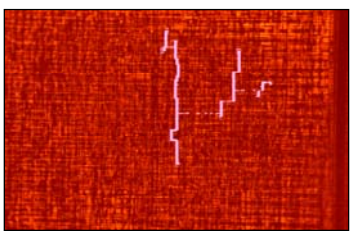
SNL Microsystems Product Infrastructure

FA/Reliability
IC Interconnect Open Identified Using CIVA

Rad Physics/ Hardness Assurance
IC Co^{60} Radiation Testing



Test/Qualification
IC Testing On Advantest 3342
QML "Like" Qualification

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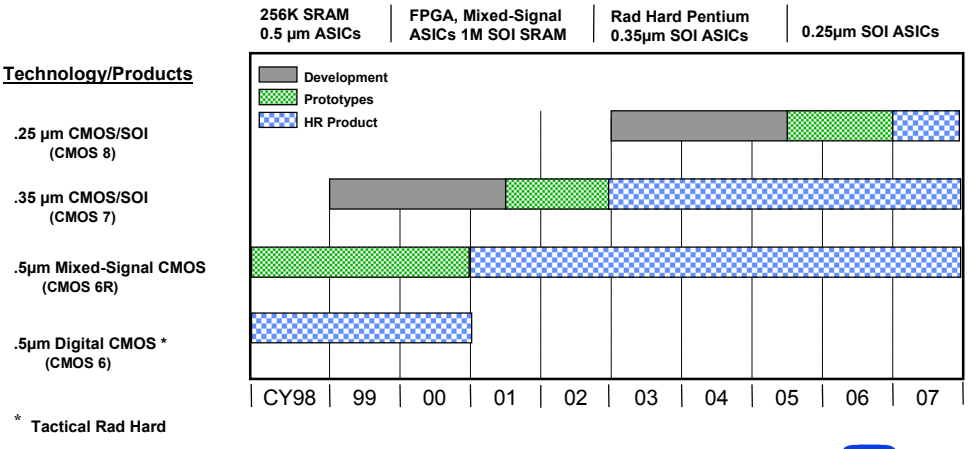
Rad Hard CMOS Technology Roadmap



* Tactical Rad Hard

December 01

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Technology Radiation Performance

Technology	Nominal VDD (volts)	Total Dose (rads(Si))	Dose-Rate Upset (rads(Si)/s)	SEU LET Threshold (MeV-cm^2/mg)	Latchup
CMOS6R (.5 µm CMOS/Bulk)	5.0	> 1M	> 10^9	> 40	None
CMOS7 (.35 µm CMOS/SOI)	3.3	> 1M	> 10^{11}	> 40	None

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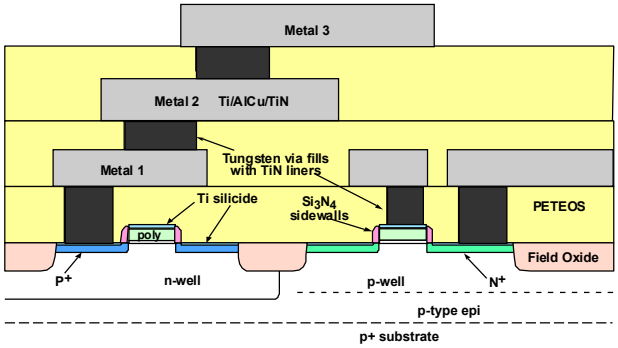
Rad-Hard 0.5µm CMOS/Bulk Technology (CMOS6R)



- 5-V CMOS, 30 ns Access Time
- Single-level, Single Work Function Polysilicon (implanted)
- RH Shallow-trench Isolation
- Titanium SALICIDE, Poly and all S/D Regions
- Planarized Interlevel Dielectrics (chem/mech polish)
- Twin wells
- LDDs
- 13-nm Gate Oxide
- Tungsten via Fills (blanket)
- SEU Resistors (50K/sq.)
- Analog Bipolar Transistor
- Analog Capacitor

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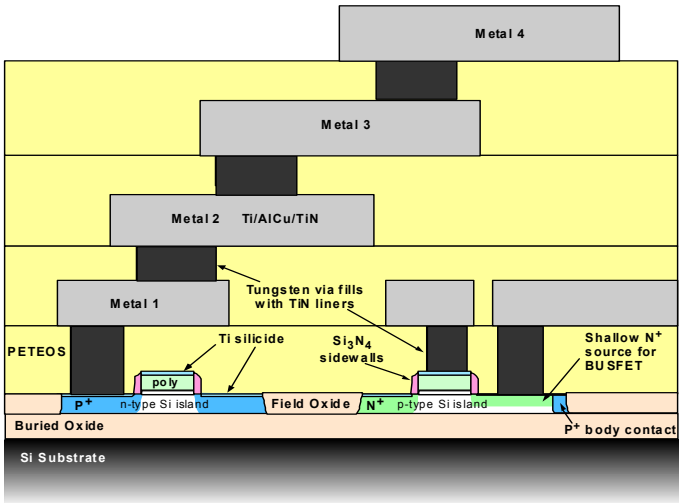
Rad-Hard 0.35µm CMOS/SOI Technology (CMOS7)



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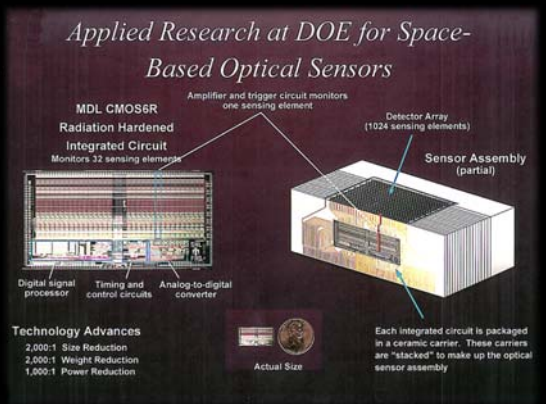
Integrated Microsystems



Focal Plane Array Sensor Module Delivered to 5700 on GPS Satellite

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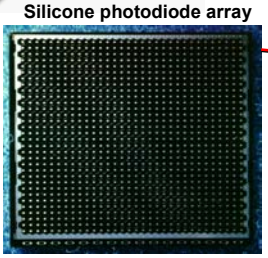
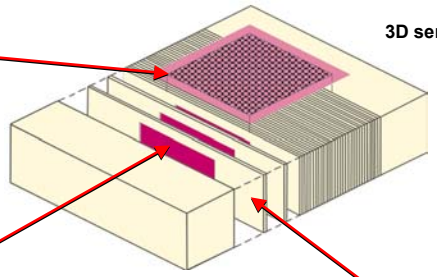
3D Microelectronics/Sensor Packaging

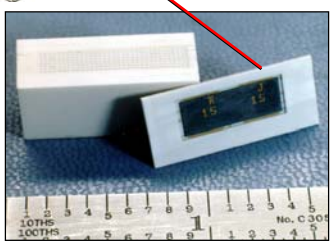
Silicone photodiode array





3D sensor assembly

Integrated circuit



8-layer prototype stack

Technology Advances

>10,000:1 Data Reduction
2,000:1 Size Reduction
2,000:1 Weight Reduction
1,000:1 Power Reduction

Analog Microelectronics

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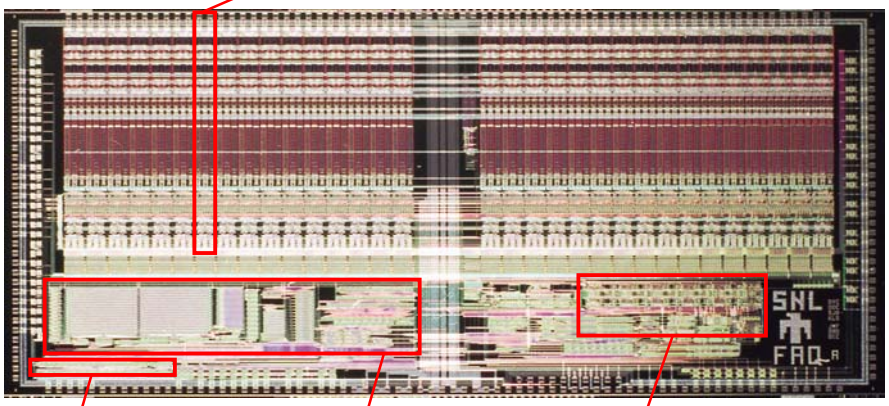
Custom Mixed Signal IC Design for "System on a Chip" Level of Integration and Performance

Low-noise, fully differential analog amplifier and threshold circuit (1of 32)



IEEE 1149 boundary scan interface and test port

16-bit digital signal processor

100-kHz, 10-bit A/D converter

Analog Microelectronics

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Focal Plane Array ASIC

- **Each sub-module of 32 die can:**
  - Simultaineously process any 7 of 256 pixels including:
    - Nulling background offset
    - Time stamp each optical event
    - Identify the pixel location
    - Digitize, filter, and >1000:1 data compression
  - Sequentially scan the background level of all pixels
  - Operate autonomously wrt power, clocks, and I/O
- **Each die includes:**
  - Low noise/power (<250 PA RMS, 2W for 1K pixels)
  - Self arbitrating MUX (32 pixels to 8 analog channels to 8 die)
  - 10 bit Log 2 A/D, 80KSPS
  - 5 MIPS, 16-bit DSP w/128x16 FIFO

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RHP Program

- The Rad Hard Pentium Program develops a 200 MIPS Class Radiation Hardened Microprocessor Chipset and Computer Module through a long-term License Agreement with Intel Corporation.
- This Program is enabled by a Government Partnership between:
  - Sandia National Laboratories (DOE)
  - Air Force Research Laboratory (KAFB and WPAFB)
  - National Reconnaissance Office
  - NASA (GFSC and JPL)

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RHP Chipset is Enabled by SNL/Intel Agreement

- Intel and Sandia have agreed to a no fee license agreement announced on 12/8/98.
- Intel Corporation will provide the design of its Pentium® microprocessor and 430HX supporting chipset to Sandia National Laboratories for development as a radiation hardened computer chipset for defense and space applications.
- The rad-hard version of the Pentium® chipset can be manufactured only in the U.S. by industry third party sources, or by Sandia.

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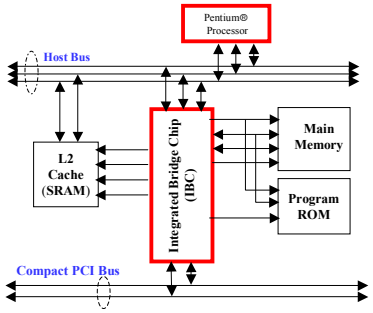
Rad Hard (Pentium® -Based) Processor Chipset & Module Development Program

Outcomes

- Readily available high-performance processor chip-set and single-board computer, based on commercial architecture, for weapon, military and commercial space applications
- Assured supply of products for low-volume user:
  - Government owned IP
  - Industry backup production
  - Sandia Design & Fab
- Leveraging popular COTS architecture to lower rad-hard system development & production cost
- Establishing a migration path from industry microprocessor technology to the rad-hard and military market

Deliverables

A 200 MIPS class radiation-hardened processor chipset and single-board computer module



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The RHP Program Has Several Unique Attributes

- The manufacturing package to the rad-hard Pentium can be licensed by the government to all qualified vendors.
- Intel, as a major player in the high-performance processor market, will work only with Sandia, based upon historical relationships, Cooperative R&D Agreements and previous successful design transfers.
- 20-Year agreement with Intel enables a migration path which will preserve investments in application software.
- SNL provides an assured source of supply, should no qualified commercial vendors be available.

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Sandia Will Perform the Following RHP Program Tasks

- Design and fabricate processor and bridge chipset using Sandia internal foundry
- Qualify Sandia foundry process for limited production and delivery of flight quality parts
- Should high volume production be needed, Sandia will transfer the Chipset Fabrication Data Package to a third-party rad-hard foundry in U.S.

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RHP Chipset Specifications Exceed Satellite Requirements

Parameters	1st Silicon Prototypes	Goal
Target Technology	.35um CMOS/SOI	
Total Dose (rads)	>300K	1M
SEU Threshold (LET)	40	60
Operating Voltage	3.3V	
Ambient Operating Temperature	-55C/+75C	-55C/+85C
Processor Operating Power (Watt)	3	5
Bridge Chip Operating Power (Watts)	1	2
Dose Rate Latchup (rad/sec)	None	None
Dose Rate Upset(rad/sec)	10^9	10^{11}
Clock Frequency (MHz)	60	120
SpecInt Performance	1.88	3.77
SpecFp Performance	1.41	2.82

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RHP Program Milestones Will Result in Prototypes during FY02

Intel Agreement	12/8/98
Project Start	1/15/99
Program PDR	10/19/99
Processor, Bridge PDR	12/00
Module Breadboard (w/FPGA Bridge)	4/01
Bridge Chip - 1st Silicon prototype	9/02
Processor - 1st Silicon prototype	12/02
Flight qualified Chipset	9/03

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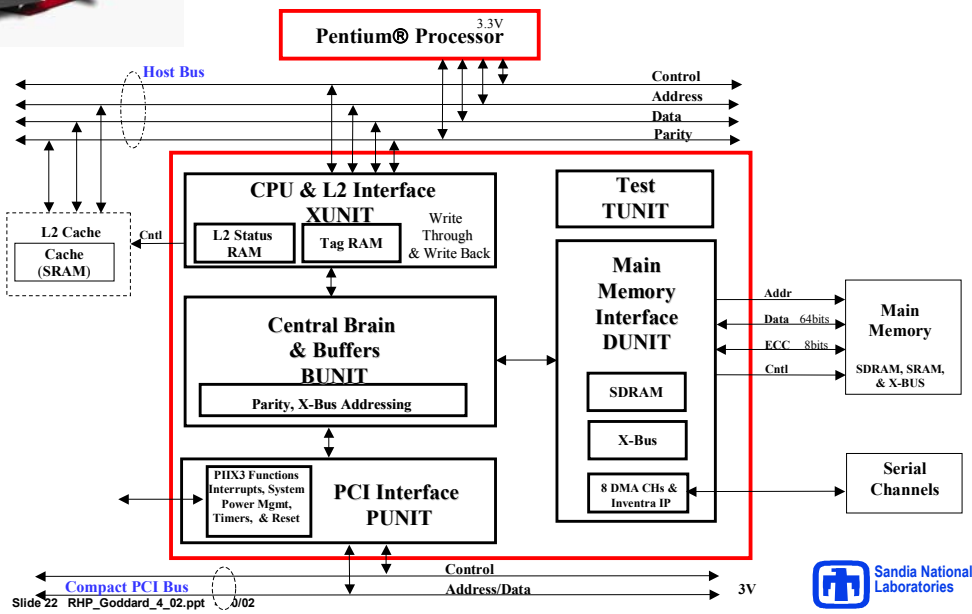
IBC Architecture



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Integrated Bridge Chip (IBC) for Pentium® Embedded Application

- Support multi-processor architecture
- Compact PCI 2.1
- M85230 Enhanced Serial Communication Controller
- 512MB total main with up to 16MB SRAM and 512MB SDRAMs
- 64bit data interface with 8bit ECC or parity
- Four full duplex USARTS, Eight independent DMACs
- Three Timers
- Interrupt Controller
- Write-through or write-back level 2 Cache Controller for 0KB, 256KB or 512KB cache

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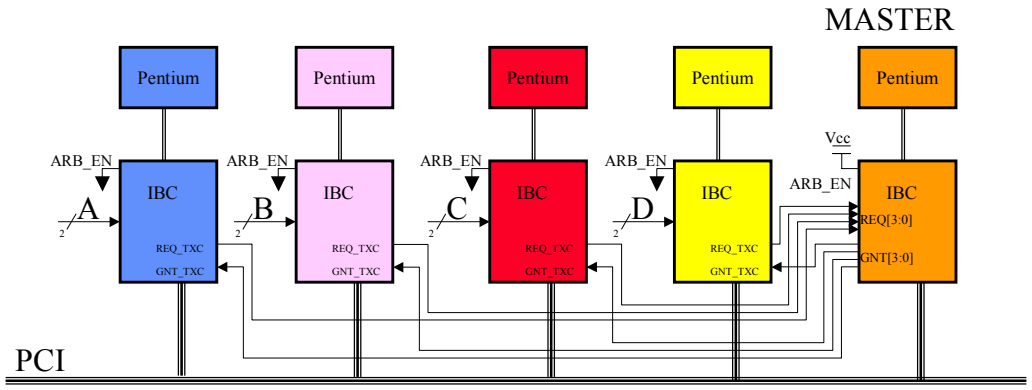
Multi-Processor Approach



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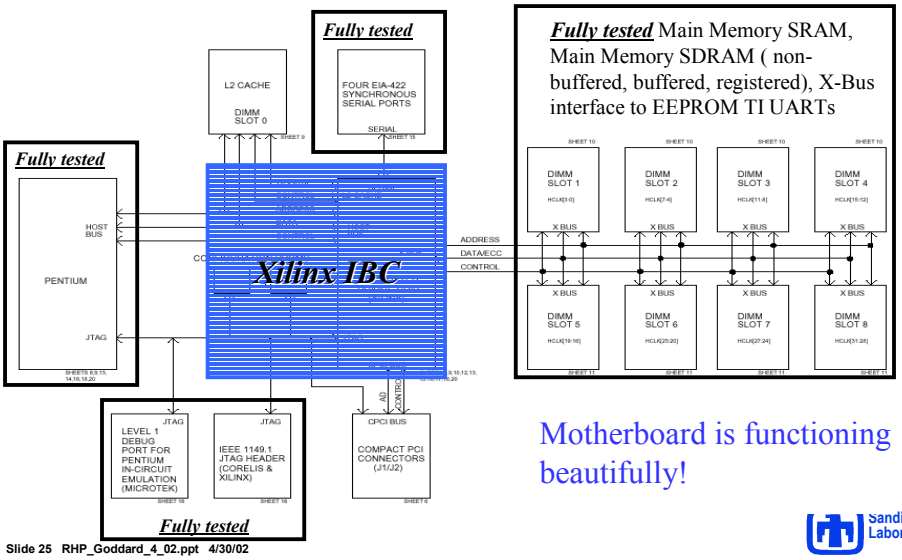
Motherboard Block Diagram



Motherboard is functioning beautifully!

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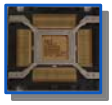
JACKSON AND TULL

Need for Cost-Effective Rad Hard Computers

- Emphasis to reduce flight hardware weight, increase processor capacity and speed while maintaining highly reliable and reasonably affordable computer systems
- Complex microsat and nanosat missions require high performance computer systems that are light-weight, small, and low power
- J&T's objective is to revolutionize flight computer system technology through standardization
  - J&T has invested its own funds to develop the flight computer
  - J&T is experienced in designing and producing flight hardware



Mongoose I
XTE and TRMM spacecraft

486 Processor
Hubble Space Telescope

JACKSON AND TULL

J&T's Approach & Collaboration with SNL

- Provide a broad solution using standard hardware and firmware rather than a point design to foster competition
- J&T's *standards-based* computer system:
  - Uses an open architecture for easier integration into existing aerospace designs
  - Is devoid of proprietary interfaces to promote competition
  - Uses existing standards in order to (1) reduce design uncertainty; (2) utilize off-the-shelf components; and (3) promote industry acceptance
  - Follows ad-hoc aerospace standards to ensure that the space computer standards meet environmental and reliability requirements
- J&T will design, integrate SNL's rad hard Pentium® (RHP) chipset, fabricate, test, and commercialize the product
- SNL will design, fabricate, and test the RHP chipset and provide test support to J&T
- A flight demonstration opportunity is being sought

The RHP Program is Progressing Well

- **Intel design database transfer done**
  - » Due to Tools & Age, database conversion & verification is difficult
  - » Access to Intel internal models, simulator, & staff are invaluable (internal observeability)
  - » Verifying Intel supplier vectors (where questions) thru Pentium hardware test
- **Integrated bridge chip design near tapeout**
  - » Converted North & South Bridge to Integrated Bridge for Embedded Applications
  - » SNL additions to Intel design (> 50%) added for embedded applications
  - » Final stages of FPGA debug, synthesis, and layout for 6/02 Tapeout
  - » Key enabler for embedded applications including SNL G&C flight computers
- **P54CS (Pentium) Chip Development**
  - » Chip Level Model has been Assembled & Continually Simulated to verify equivalency
  - » Chip is a combination of synthesis & custom design vs. Intel primarily custom
  - » RH design conversion and Layout is underway
  - » RHP Test Capability Established through purchase of Intel IMS Tester/Hardware
- **Breadboard Module hardware and software demonstrated**
  - » FPGA bridge chip emulation (commercial Pentium & IBC FPGA) operational & invaluable in debugging design

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Summary

- Sandia Systems need custom and rad hard μE
  - Industry suppliers are at risk
- Sandia's Microelectronics facilities provide μSystems R&D and Products for SNL & Govt. Applications
- RHP and Bridge Chips will be available this year